REMARKS

Applicant's representative (Matthew H. Szalach, Reg. No. 53,665) would like to thank Examiner Sandvik for the courtesies extended during a telephonic interview on June 16, 2006. During the interview, the Examiner clarified the rejection of independent Claims 1, 11, 12, and 13 under 35 U.S.C. § 102(e). Specifically, the Examiner noted that while Nishimura (U.S. Patent No. 6,781,241) fails to teach a gap or void disposed between a second carrier substrate and a first semiconductor chip, that Degani (U.S. Publication No. 2002/0079568) discloses such a gap. Applicant has cancelled independent Claims 11, 12, and 13 and submit herewith an amended independent Claim 1 that is believed to define over Nishimura and Degani.

Claims 1, 3-5, 8, and 10 are now pending in the application. By this paper, Claim 1 has been amended and Claims 11-13 have been cancelled without prejudice or disclaimer of the subject matter contained therein. The basis for these amendments can be found throughout the specification, claims, and drawings originally filed. No new matter has been added. The preceding amendments and the following remarks are believed to be fully responsive to the outstanding Office Action and are believed to place the application in condition for allowance.

The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 3-5, 8, 10, 11, and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nishimura et al. (U.S. Patent No. 6,781,241).

Claim 12 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Degani et al. (U.S. Publication No. 2002/0079568).

These rejections are respectfully traversed.

At the outset, Applicant respectfully submits that this rejection is moot with respect to Claims 11-13, as Claims 11-13 have been cancelled without prejudice or disclaimer of the subject matter contained therein. Reconsideration and withdrawal of the rejection is respectfully requested.

Independent Claim 1 recites a semiconductor device including a first carrier substrate, a first semiconductor chip mounted face down on the first carrier substrate, and a first anisotropic conductive sheet disposed between the first semiconductor chip and the first carrier substrate. The first anisotropic conductive sheet includes a first side and a second side with the first side being in contact with the first carrier substrate and a pair of lands and the second side having a first portion in contact with the first semiconductor chip and a second portion that extends past the first semiconductor chip. A second carrier substrate is held above and spaced apart from the first semiconductor chip such that a gap is created between the second carrier substrate and the first semiconductor chip and between the second carrier substrate and the second portion of the first anisotropic conductive sheet.

Nishimura fails to disclose an anisotropic conductive sheet disposed between a semiconductor chip and a carrier substrate. Therefore, Nishimura also fails to disclose an anisotropic conductive sheet having a first side in contact with a carrier substrate and a second side having a first portion in contact with a semiconductor chip and a second portion extending past the semiconductor chip. Applicant also respectfully submits that

Nishimura fails to disclose a gap formed between a portion of an anisotropic conductive sheet and a second carrier substrate held above and spaced apart from the anisotropic conductive sheet.

Nishimura teaches a stacked-type semiconductor device including a first carrier substrate (1b) having a first semiconductor chip (3b) disposed on a top surface thereof and a second semiconductor chip (3f) disposed on a bottom surface thereof generally opposite from the top surface. See Nishimura at Col. 5, Ins. 12-24, and Figure 6. Nishimura further teaches a second carrier substrate (1a) having a plurality of stacked semiconductor chips positioned thereon (3c, 3d). See Nishimura at Figure 6. The second carrier substrate is positioned generally above the first carrier substrate and is bonded thereto by a series of solder balls (7). See Nishimura at Col. 5, Ins. 18-21, and Figure 6. Nishimura is silent with regard to including an anisotropic conductive sheet disposed between any of the semiconductor chips and the substrates on which the semiconductor chips are supported. In light of the foregoing, Applicant respectfully submits that independent Claim 1, as well as Claims 3-5, 8, and 10, dependent therefrom, are in condition for allowance. Reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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